WHAT IS CLAIMED IS:

1. A semiconductor storage device comprising:

a memory cell including a capacitor and a pass transistor, wherein the capacitor includes a capacitive film made of a ferroelectric and the pass transistor is connected to a storage node of the capacitor;

a sub bit line connected to the pass transistor;

a gain transistor whose gate, drain and source are connected to the sub bit line, a bit line, and a source line, respectively; and

a charging device for charging the voltage of the sub bit line up to the threshold voltage of the gain transistor or a voltage value obtained by adding an offset to the threshold voltage.

2. The device of Claim 1, further comprises a reset-voltage applying device for applying a predetermined reset voltage to the sub bit line.

3. A method for driving a semiconductor storage device, wherein the semiconductor storage device includes: a memory cell which includes a capacitor having a capacitive film made of a ferroelectric, and a pass transistor connected to one electrode of the capacitor; a sub bit line connected to the pass transistor; a gain transistor whose gate, drain and source are connected to the sub bit line, a bit line and a source line, respectively; and a charging device for charging the voltage of the sub bit line up to the threshold voltage of the gain transistor or a voltage value obtained by adding an offset to the threshold voltage, the method comprising the steps of:

(a) charging, by the charging device, the sub bit line and said one electrode of the capacitor up to the threshold voltage or the voltage value obtained by adding the offset to

the threshold voltage, and

(b) applying a read voltage to the other electrode of the capacitor for detection of variation in channel resistance in the gain transistor, thereby reading out data retained in the capacitor.

4. The method of Claim 3, wherein the semiconductor storage device includes a reset-voltage applying device for applying a predetermined reset voltage to the sub bit line, and

the step (a) further includes the step of turning on the reset-voltage applying device so that the reset voltage is applied to the sub bit line, and thereafter turning off the reset-voltage applying device.

5. The method of Claim 3, wherein the step (a) further includes the step of applying, to the other electrode of the capacitor, a voltage which is an intermediate voltage between the read voltage and the threshold voltage or between the read voltage and the voltage value that is obtained by adding the offset to the threshold voltage, and

the voltage applied across both the electrodes of the capacitor does not exceed the coercive voltage of the capacitive film.

6. The method of Claim 3, wherein the memory cell includes a pair of capacitors each including a capacitive film made of a ferroelectric, and

the method further includes, after the step (b), the step (c) of applying, to one of the capacitors in which the amount of polarization is varied by the read operation, a voltage for rewriting which is smaller than normal write voltage which causes said amount of polarization to be saturated.

7. A semiconductor storage device comprising:

a memory cell including a capacitor and a pass transistor, wherein the capacitor includes a capacitive film made of a ferroelectric and the pass transistor is connected to a storage node of the capacitor;

a sub bit line connected to the pass transistor;

a gain transistor whose gate, drain and source are connected to the sub bit line, a bit line, and a source line, respectively; and

a current shutoff device for shutting off drain-source current in the gain transistor.

8. A method for driving a semiconductor storage device, wherein the semiconductor storage device includes: a memory cell which includes a capacitor having a capacitive film made of a ferroelectric, and a pass transistor connected to one electrode of the capacitor; a sub bit line connected to the pass transistor; a gain transistor whose gate, drain and source are connected to the sub bit line, a bit line and a source line, respectively; and a current shutoff device for shutting off drain-source current in the gain transistor, the method comprising the step of:

(a) applying a read voltage to the other electrode of the capacitor, and shutting off the drain-source current by the current shutoff device while the potential of the sub bit line varies.

9. The method of Claim 8, wherein the memory cell includes a pair of capacitors each including a capacitive film made of a ferroelectric, and

the method further includes, after the step (a), the step (b) of applying, to one of the capacitors in which the amount of polarization is varied by the read operation, a voltage for rewriting which is smaller than normal write voltage which causes said amount of

polarization to be saturated.